THE ELECTRONICS OF THE NEW H1 LUMINOSITY SYSTEM

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In the scope of the upgrade of the HERA collider, the H1 luminosity system was rebuilt anew. The analog electronics has been designed to transmit photo-multiplier pulses with a repetition rate of 10.4 MHz through 125 m cables, to compensate for the cable skewing and to do a fast shaping avoiding pile-up. The corresponding acquisition is based on custom digitizing cards using the 41 MHz, 12 bits AD9042 ADC chip, a custom 48 Mb/s readout bus, and a commercial computing board (MFCC from C.E.S.) performing fast histogrammation of data. Preliminary results show the ability to readout data at a rate of 0.6 MHz and process them at 0.4 MHz.

1. Introduction

At HERA, the luminosity is determined by measuring the flux of bremsstrahlung photons emitted at zero degree off electrons in the field of protons. For H1, the detection is realized by a new 2×12-strip quartz fiber calorimeter, called Photon Detector (PD), situated 104 m downstream the interaction region[1] and detailed at the previous session of this conference cycle[2]. A small 12-channel calorimeter, the Electron Tagger (ET), at 6 m completes the system.

The HERA upgrade realized in 2001[3] increases the luminosity by a factor 5 and implements the longitudinal polarization for the experiments. The measurement of the luminosity then requires[4] to record the complete deposited energy spectrum, rather than mere rates, on a bunch by bunch basis and once per minute to match the 20 minute build-up rate of polarization.

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In that scope the new quartz fiber PD presents some very appealing features such as fast signal, insensitivity to synchrotron radiation photons and very high radiation hardness. It nevertheless challenges the front-end electronics because of its low light yield (about 130 photo-electrons per GeV). Due to the high bremsstrahlung rates - a significant signal is expected every 96 ns, the HERA bunch crossing (BC) period - the photo-multipliers (PM) have to be run at low gain (a few 10^5). Moreover, transmission of the pulses through 125 m cable implies attenuation and distortion which have to be compensated.

Front-end cards have been designed to scope with these problems and are first described. The associated acquisition hardware and performances are addressed in section 3 and 4 respectively.

2. Analog Electronics

The main features required from the analog electronics are to provide a substantial gain to the signal and to avoid the pile-up of signal from successive BC while keeping a 12-bit dynamical range. Its two parts, a pre-amplifier card at the back of the detectors and a shaper card in the experimental hall have been realized by the electronics group of the LAL, Orsay.

2.1. *Pre-Amplification*

The output of the PM is fed by a 20 cm-long 50 Ω LEMO cable to the pre-amplifier card, with an impedance match at both ends. A gain of 10 on a 50 Ω load is provided and allows to run the PM with a reduced gain. A card processes 14 channels (two being spare ones), provides their analog sum and a reference channel (for subtraction) in order to reduce the picked-up noise. Three such cards serve the X and Y projection of the PD and the ET.

The mechanical design has been optimized to facilitate the maintenance and to minimize the time spend in the tunnel in exchanging the card: its small dimensions ($10 \times 15\,\mathrm{cm}^2$) and the placing of the I/O on opposite faces allows it to be fixed on the door of the casing containing the PM tubes and to achieve an efficient shielding.

2.2. *Correction & Shaping*

The signals are transmitted to the shaper cards through 125 m of RG58 (low loss CERN type) coaxial cable. The 10 ns-width signal emitted by the pre-amplifier card (fig. 1a) is skewed by the transmission with the higher frequencies damped relative to lower ones, resulting in an amplitude loss of 10 dB and a prolongated tail (fig. 1b), largely exceeding the BC period.

The 16-channel card design includes *i*) two Pole Zero Compensation (PZC)

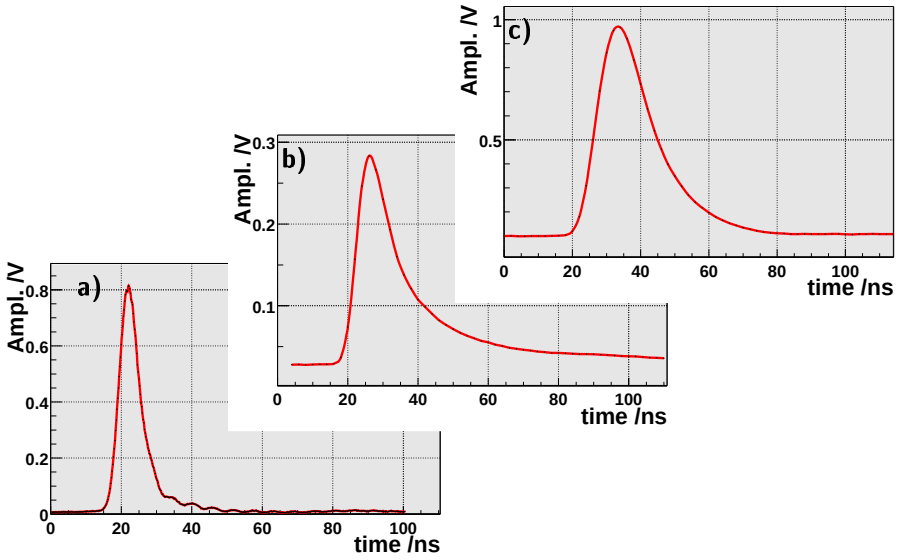

Figure 1. Evolution of an optical calibration signal, very similar to a physical one, a) at the output of the pre-amplifier card, b) after 125 m of coaxial cable, c) at the output of a shaper card.

tuned on the measured skewness of the cable, restoring fully the initial pre-amplified signal, *ii*) a unipolar shaping with a typical rising time of ∼8 ns and a return below 1 % within 72 ns (fig 1c.), *iii*) the subtraction of the reference channel. By these means, a reduction of the low frequency coherent noise, dominant at 150 Hz, from ∼80 mV to ∼8 mV is achieved, the residue originating from the local noise pick-up.

The white intrinsic noise at the shaper output is of $\sigma \sim 0.55$ mV on single channels and of 0.96 mV on the sums, pointing to a dominant component coming from the shaper card. The linearity of both cards were measured on test bench to be better than 1 %.

3. Acquisition

Due to the new requirements recalled in the introduction a completely new acquisition, parallel to the H1 central readout (running at ∼50 Hz), has been designed and realized, featuring: *i*) a fast readout and histogramming (at typically 1 MHz) of the analog sums, aiming the percent statistical precision on individual BC per minute, *ii*) a complete readout (at typically 100 kHz) of all the channels for detailed off-line analysis, *iii*) a slow control permanent monitoring of the systematics in order to keep the energy calibration at the

1 % level. In addition, stability of the sampling position with respect to the shaped pulse (fig 1c) requires precise timing monitoring.

The acquisition system is physically based on custom designed VME-sized cards and an extended VME crate; it includes 8 ADC and 1 TDC cards, a fast readout bus, named lumi bus, and a commercial mezzanine computer board, the MFCC. A Service Module provides all the external signals (clocks, triggers, ...). The full system is globally cadenced at 10.4 MHz, the frequency of the HERA clock (HCk).

Each component is described in detail in the following sections.

3.1. *ADC & TDC Cards*

The ADC cards are based on a chip AD9042 from Analog Device able to digitize a differential signal in the range 0-2 V in 12 bits at frequencies as high as 41 MHz. One card treats 8 channels in parallel, with 4 samplings per BC.

The data produced are stored independently in two pipelines of 512 pairs of sample (256 BC), each driven by its own Pipeline Enable (PEn) line; one pipeline is readout through the VME and used by the central H1 readout. The other one is readout via the dedicated lumi bus for the local acquisition.

A digital comparison on the 4 samples of two channels on the card provides the signals for triggering the local acquisition.

The TDC card is based on a chip developed for the BaBar collaboration by the team of the LPNHE, Paris, who designed the ADC and TDC cards. Each chip records as many as 16 inputs with a resolution of 0.5 ns inside a programmable time window anterior to the trigger signal. Up to 8 formated events per channel are kept at a time in an internal buffer.

One TDC card processes 8 digital and 8 internally discriminated analog inputs, digitized by 2 chips in order avoid buffer overflowing. On an external trigger, the internal buffer of the TDC chips are transfered to an external FIFO for a delayed readout, using either of the buses.

3.2. *The Lumi Bus*

The lumi bus support is a backplane board extending on 14 slots of the VME crate and connecting the J2 "A" and "C" rows. The lines have a 50 Ω impedance and critical control lines have matched terminations.

The bus, fully controlled by the MFCC, contains 24 data and 16 address and sub-address synchronous lines, cadenced at 20.8 MHz (2 × HCk), plus several asynchronous control lines (Reset, Synchronization, Pipeline Enables, TDC trigger, ...). The addresses and data bits are offset by one clock cycle in order to improve the performances.

3.3. *The MFCC Acquisition Board*

In form of a mezzanine board, the MFCC 8441 (Multi-Function Computing Core), a commercial product developped by C.E.S.[5] for communication, is a fully developed computation unit based on a 300 MHz PowerPC, 32 MB of RAM, a 66 MHz bus and two fast FPGA (Altera 10K50). One of them ensures the communication with the carrying VME station (via a PCI bus). The other one is dedicated to lumi bus control and data I/O.

In this "user" FPGA, the following tasks are realized:

- Trigger Logic: 16 maskable bits originating from the ADC cards can launch a readout sequence (standard "triggered" mode). The start can also be given by a specified BC number and allows to record a number of consecutive BC in a row ("train" mode).
- Synchronization: internal counters for the BC number and the ADC pipeline index (commanded by the "lumi" PEn) are kept up to date.
- Readout Sequencing: on a readout command, the addresses and subaddresses are send on the bus. They are formed from the required mode ("triggered" or "train") sequence table, modifiable by the PowerPC on the fly, and from the pipeline index.
- Data Formatting & Output: the corresponding data fetched from the ADC cards are completed by the local information (BC number, trigger bits, ...), formatted and put into the FIFO using the internal dual port memory of the FPGA. The latter provides the buffer needed between the 20.8 MHz input and the 66 MHz output.

The "train" mode, limited to 55 BC by the FIFO size, allows to accumulates rapidly a high statistic on the analogically summed energies and avoid completely any trigger screening effect, an otherwise overwhelming problem at high luminosity. A full HERA cycle (220 BC) is completed with 4 such trains.

4. Preliminary Performances

The data available in the FIFO of the user FPGA are processed by a standalone program (no OS) on the MFCC PowerPC and histogrammed.

The present acquisition time in "train" mode is of 2.5 μs/BC (readout only: 1.6 μs/BC). Limited by the CPU (192 ns expected from bus, 460 ns from sequencing chaining), it will be improved by software optimization. A typical distribution obtained is shown on figure 2. In the "triggered" mode the total energy is calculated from individual channels at a rate of 27 kHz.

Once per second the histograms are sent to the carrying board for analysis, extraction of the luminosity numbers and checking of the calibration.

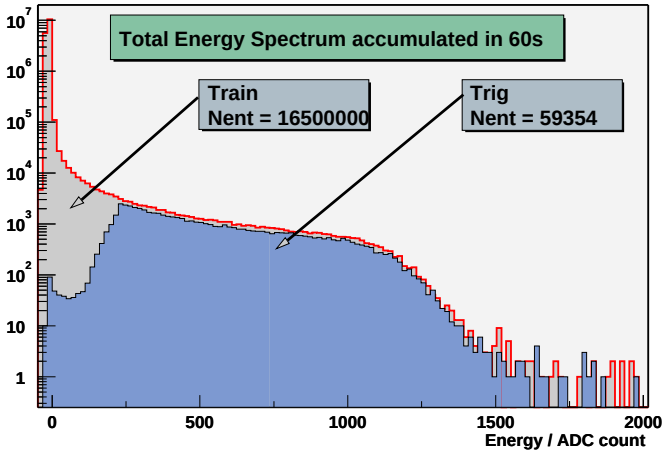

Figure 2. Typical bremsstrahlung spectrum accumulated on the Y projection of the PD in one minute by 60 interleaved "train" (clear) and "triggered" (dark) acquisitions (see text), reading respectively the analog sums and all the channels. Pure processing rates were of 400 kHz and 27 kHz.

Conclusion & Perspectives

A completely new electronics ranging from pre-amplification to acquisition has been realized and is fully operationnal for the new H1 luminosity system. A 12-bit dynamical range for analog pulses is currently provided at the end of 125 m cables. The acquisition developped allows currently to process the 42 MHz digitized data at a rate of 2.5 μs per bunch crossing on a train of 55 successive bunches and to read full events for the control of the systematics.

Since the conference the system has been commissioned and is now (June 2002) in operation while HERA is tuning the beams for luminosity production. The very same electronics and acquisition is used for the transverse and future longitudinal polarimeter of HERA.

References

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